Accurate behavioral modeling technique for simultaneous active multiple LVDS line drivers

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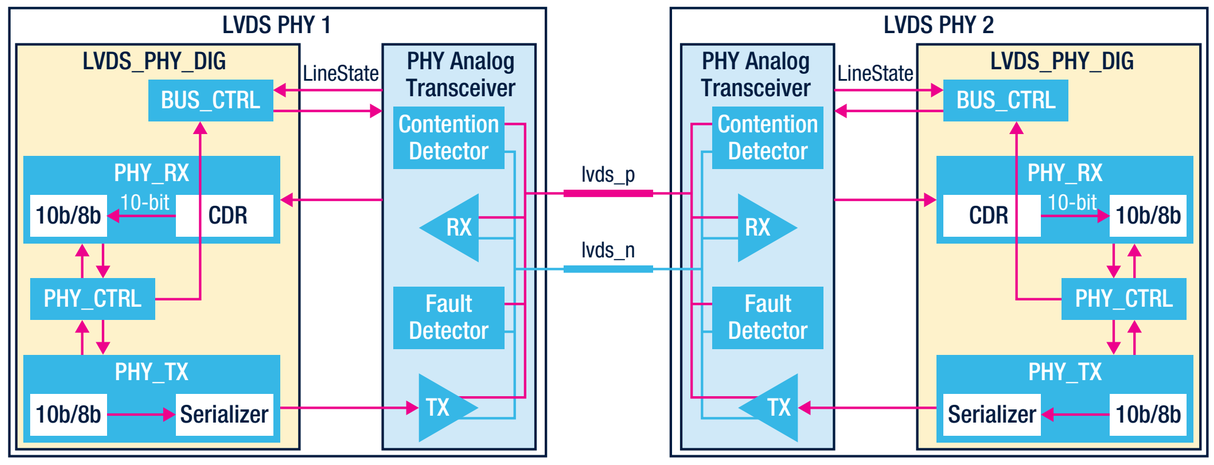
1. MOTIVATION

Design architecture:

- LVDS PHY with analog transceiver and digital PHY layer with half-duplex point-to-point communication
- Bus contention detection and contention resolution when the data transfer is initiated from both sides (PHY1 & PHY 2) simultaneously.

Modeling challenge:

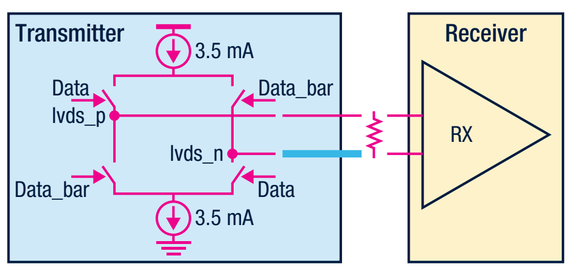
- Behavioral modeling of LVDS exists, but it is not sufficient to support this kind of bus contention.
- Since two-line drivers operate on the same channel, the arbitration algorithm of a model must be developed to handle such contention.



To overcome the above challenges, a new methodology using user-defined net types and resolution function is developed and deployed.

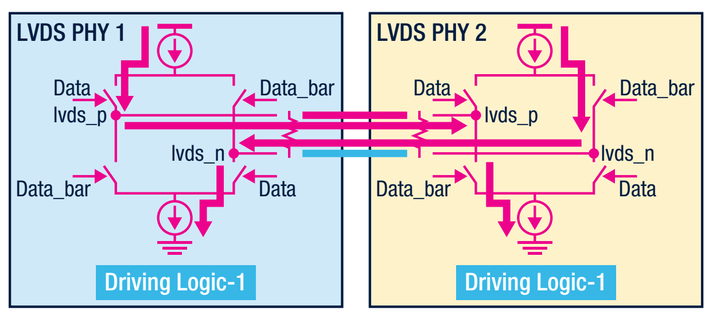
2. LVDS OPERATION & CONTENTION AND VERILOG MODELING USING STD. LOGIC

Low voltage differential signaling operation



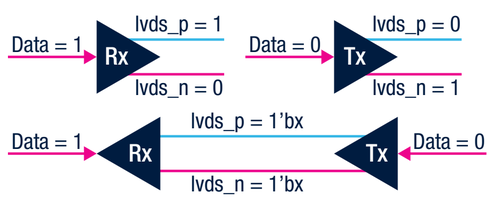
- LVDS is a current mode driver.
- Current passes through the receiver termination resistance and returns to driver generating the differential voltage.
- Four switches on the transmitter side control the direction of the current, depending on the logic level of the data bit to transmitted.

Contention



- Contention is if two connected PHY try to transmit data simultaneously.
- When both are driving the same logic (0/1), then output will settle at that logic.
- If both PHY are driving opposite logic, then no current will pass through the termination resistance, resulting in zero potential difference between lvds_p and lvds_n.

Verilog modeling using std. logic



- In std. logic modeling,
  - For logic-1, lvds_p = 1'b1 & lvds_n = 1'b0.
- In the case of contention,
  - Both PHY drives same logic, output will be resolved.
  - But when both PHY drives opposite logic, the output will be 1'bx.
- Contention modeling using the std logic behavioral model is therefore not possible.

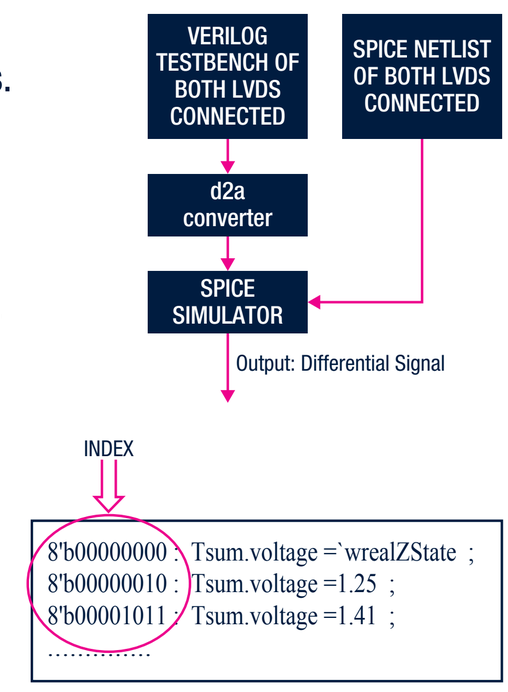
3. PROBLEMS IN RNM & PROPOSED MODELING TECHNIQUE

Problem in RNM:

- Problem: output from Verilog does not match with the spice values.
- Example: 1 PHY transmitter is ON & termination resistance of both PHY is off
  - The output in SPICE will be rail to rail
  - But output from Verilog will be independent of power supply.
- Adding more variables like power supply will reduce its scalability.

Proposed modeling technique:

- Proposed solution is based on look-up (LU) table resolution function
- LU table can be extracted using mixed signal simulation for all the configurations.
- For 2 PHY, two variables, mode_0 and mode_1, are used.
  - mode_1[3]: transmitter is enabled or not.
  - mode_1[2]: strength of the transmitter.
  - mode_1[1]: logic level transmitter is trying to send.
  - mode_1[0]: status of termination resistance.
- With mode_0 and mode_1, 8 bits of data available to determine differential voltage.
- Each bit of mode_0 and mode_1 corresponds to the logic of pins in LVDS. We can develop a Verilog test bench.
- Mixed-signal simulation with the Verilog testbench and SPICE netlist of LVDS can be used to extract the DC voltage levels of lvds_p and lvds_n at each possible configuration of ({mode_0, mode_1}) to generate a LU table.



4. RESULT & CONCLUSION

- Look-up table-based resolution is more suited to validate behavioral model against the spice behavior.

- The above figure above shows the comparison between the Verilog and the SPCIE voltage waveforms. As evident from the waveforms, Verilog, in blue and SPICE voltages, in red, are closely matched.
- As behavior modeling is technology independent, this extensive look-up table-based resolution function has been used and verified for other LVDS in different technologies as well.

Future scope

- Automation can be used to convert extracted data from mixed-signal simulation to LU table.
- LU table-based resolution function is scalable to the cases where more than two LVDS are connected and to the other current-mode drivers as well.